Power-Efficient Pulse Width Modulation DC/DC Converters with Zero Voltage Switching Control

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ABSTRACT

This paper proposes a power-efficient PWM DC/DC converter design with a novel zero voltage switching (ZVS) control technique. The ZVS control is realized by an inner feedback loop which is implemented by simple digital circuitry between the input and output of the power transistors and achieves real-time zero voltage switching (ZVS) for various loading and device parameters with power efficiencies over 90.0%. In addition, an outer feedback loop is used to ensure that the output precisely tracks a reference voltage level. We have also built the relationship between the output voltage ripple and the speed of the voltage comparators which has shown to introduce new low-frequency signals to the loops and cause significant output voltage ripples. Experiment results show that the output ripple could be reduced by 4x by carefully handling the generation and propagation of these low frequency signals.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles

General Terms

Design.

Keywords

DC/DC conversion, zero voltage switching.

1. INTRODUCTION

Power consumption has become one of the most important issues in modern electronics due to increased complexity and speed of the system. In order to curb the effect of power on a system as a whole, multiple power domains have been proposed as an architecture scheme for low power design. To support multi-Vdd, an array of supply voltages need to be generated. DC/DC converters can be integrated on chip and convert the input voltage to different voltage levels internally. Recently, a great deal of research [1–5] has been devoted to improving the power efficiency and reducing the area cost of on-chip DC/DC converters. However, there are still many unsolved problems. For instance, the basic linear regulator and the charge-recycling voltage regulator are designs that have been looked at as candidates for on-chip integration because there are no filter elements. However, the relative low power efficiency, typically less than 80% [1], of these designs has limited their application.

In this paper, we propose design techniques and analysis to address the above problems for high frequency PWM buck converters. We first introduce a real-time ZVS technique which relies on a feedback loop as opposed to tuning device parameters to achieve ZVS during design time as in traditional methods [4]. Our experiment results show that the feedback mechanism guarantees ZVS under different loading and device parameters. Furthermore, using the real-time ZVS technique we are able to achieve power efficiencies over 90.0%. We then study close loop design and analysis of PWM buck converters. Our experiment results show that output voltage ripple in a closed loop PWM buck converter can be reduced up to 4x by correctly analyzing and optimizing the sources that generate and propagate low frequency signals.

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2. BACKGROUND AND DESIGN OVERVIEW

2.1 Principles of PWM Buck Converters

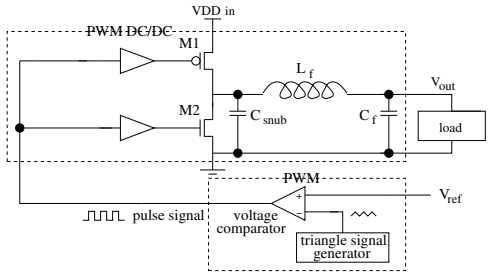

Figure 1: Schematic of a PWM buck converter.

Compared to other designs, such as linear regulators, PWM buck converters consume more area but have higher power efficiency. The schematic of a PWM buck converter is shown in Fig. 1. It consists of two power transistors, $M1$ and $M2$, with their drivers, a low-pass LC filter consisting of L_f and C_f, a snubber capacitor C_{snub}, and a pulse width modulator.

The output voltage level V_{out} is the DC component of the pulse signal generated by the PWM, and it is

$$V_{out} = Vdd_{in} \cdot D, \tag{1}$$

where D is the duty cycle of the pulse signal, which is con-

trolled by V_{ref} as an input of the PWM. In fact,

$$D = \frac{V_{ref}}{Vdd_{in}}. \quad (2)$$

Therefore, we have

$$V_{out} = V_{ref}. \quad (3)$$

As shown in [6], the output voltage ripple of a PWM buck converter can be expressed as

$$\Delta V_{out} = \frac{Vdd_{in}(1-D)D}{8L_fC_ff^2}, \quad (4)$$

where L_f and C_f are the inductance and capacitance of the LC filter and f is the frequency of the pulse signal. f is also called the operation frequency of the buck converter.

Equation (4) shows that to keep ΔV_{out} at a low level, L_f and/or C_f has to be large if the operation frequency f is low. In other words, an effective way to reduce the area of the LC filter in the buck converter is to use a high operation frequency [2]. However, a high operation frequency leads to a high switching power loss. To reduce the switching power loss, a technique called zero voltage switch (ZVS) has been widely adopted. As shown in [4], ZVS ensures that both power transistors switch under a zero voltage drop between source and drain.

2.2 Overview of the Proposed Topology

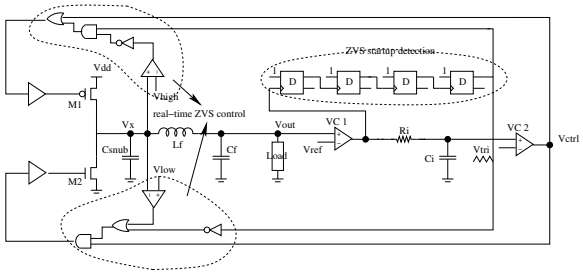

Figure 2: Overview of the proposed circuit topology.

Our study in this paper is based on the circuit topology shown in Figure 2. This circuit contains two feedback loops. The outer loop consists of two power transistors M_1 and M_2, LC filter L_f and C_f, voltage comparator $VC1$, RC integrator R_i and C_i, pulse modulation element $VC2$, and real-time ZVS circuitry. The inner loop starts from the output of the two power transistors, passes through the ZVS circuitry and ends at the input of the two power transistors.

The outer loop ensures that the output voltage level V_{out} tracks the reference voltage level V_{ref}. It is considered a negative feedback loop since there are only one set of negative components, the power transistors, in the entire looop. For example, if V_{out} is higher than V_{ref}, the output of voltage comparator $VC1$ is high, C_i is charged, and the voltage level at the positive input of $VC2$ is increased, which increases the duty cycle of the switching signal and therefore decreases V_{out}.

The design of voltage comparator is adopted from [7], which has shown high resolution and low power consumption. The topology of the voltage comparator is shown in Figure 3, which is composed by an input amplification stage, two flip flops and a RS latch. Two clock signals are used to clear up previous results and evaluations. More details are described in [7].

The real-time ZVS technique is achieved by the inner feedback loop. To avoid the influence of startup strike, a detection sub-circuit is included as shown in Figure 2. The idea is not to startup the ZVS circuitry until V_{out} has been stabilized. More details will be described in Section 4.

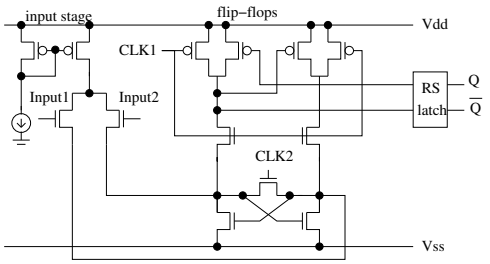

Figure 3: Topology of the voltage comparator.

3. CLOSE LOOP DESIGN AND ANALYSIS

3.1 Analysis on output voltage ripple

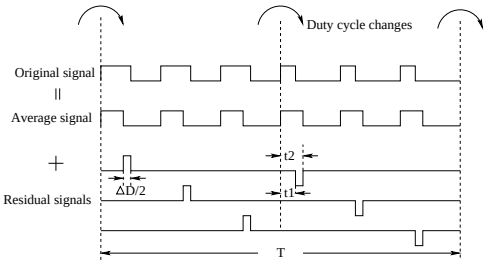

Figure 4: Illustration of changes in duty cycle in the switching signal.

Our study is based on the design shown in Figure 2. The voltage comparator VC_2 in the figure modulates the duty cycle of the switching signal feeding the two power transistors and this modulation introduces a signal that contains a wide range of frequencies. Low frequency components of this signal may pass the LC filter and cause a voltage ripple with a frequency approximately equal to the frequency of the LC filter,$1/(2\pi\sqrt{L_fC_f})$, at the output terminal. Note that the voltage comparator VC_1 may also bring in low frequency components but it is filtered by the R_iC_i integrator and has a smaller impact to the overall output ripple.

Figure 4 illustrates the behavior of the operating switching signal during steady state. In the figure, this signal is decomposed into an average signal, which maintains a constant duty cycle and a set of residual signals. The average signal contains only high frequency components, and the residual signals contain a wide range of frequency components. The duty cycle switches between two states D_1 and D_2 has a frequency the same as the output voltage ripple, which is roughly equal to frequency of the LC filter, i.e.,

$$T = 2\pi\sqrt{L_fC_f}. \quad (5)$$

By Fourier transformation, the residual signals can be expressed as follows,

$$\begin{aligned} f(t) =& \frac{2V_{dd}}{\pi}[\sum_{n=0}^{\infty}(\frac{sin(2n+1)\omega t_2 - sin(2n+1)\omega t_1}{2n+1})cos(2n+1)\omega t \\ &+ \sum_{n=0}^{\infty}(\frac{cos(2n+1)\omega t_1 - cos(2n+1)\omega t_2}{2n+1})sin(2n+1)\omega t] \\ =& \frac{2V_{dd}}{\pi}\sum_{n=0}^{\infty}\frac{\sqrt{2-2cos(2n+1)\omega(t_2-t_1)}}{2n+1}cos((2n+1)\omega t+\phi) \\ \approx& \frac{2V_{dd}}{\pi}\sum_{n=0}^{\infty}\omega(t_2-t_1)cos((2n+1)\omega t+\phi), \end{aligned}$$

where

$$\omega = \frac{1}{\sqrt{L_f C_f}}. \quad (6)$$

Notice that $t_2 - t_1 = T \cdot \frac{\Delta D}{2}$, we have

$$f(t) = \frac{V_{dd} T}{\pi \sqrt{L_f C_f}} \Delta D \sum_{n=0}^{\infty} cos((2n+1)\omega t + \phi). \quad (7)$$

From (6) we can see that ω is the 3db frequency of the LC filter which implies that the magnitude of a signal at this frequency becomes half when it passes through the LC filter. Also, equation (7) implies that the residual signals contain frequency components of ω, 3ω, $\cdots$, etc and the magnitudes of these components are proportional to ΔD. Given that ω is the 3db frequency of the LC filter, when the residual signals enter into the LC filter, the low frequency components, such as ω, 3ω and 5ω, can pass through the LC filter with significant magnitudes and appear as a ripple at the output terminal. Because the magnitudes of the low frequency components of ω, 3ω and 5ω etc. are proportional to ΔD, the magnitude of the ripple is proportional to ΔD too. Practically every voltage comparator has a smallest value of ΔD. In slower voltage comparators this ΔD are generally larger than in faster comparators. Therefore, we suggest to use fast voltage comparators to avoid large ripple at the output.

4. REAL-TIME ZVS TECHNIQUE

4.1 Traditional ZVS techniques

A representative traditional design-time ZVS technique without feedback is presented in [4]. To illustrate the ZVS conditions, each cycle of the internal switching signal is divided into four time fragments, T_1, T_2, T_3 and T_4 in the figure. During T_1 and T_3, the NMOS power transistor M_2 and PMOS power transistor M_1 close, respectively. During T_2 and T_4, both transistors are open. These two time fragments are called deadtimes. V_x drops to zero at the beginning of T_1 when M_2 starts to close. Also, V_x reaches Vdd when M_1 starts to close. Thus, M_1 and M_2 switch at a zero voltage drop between the source and drain i.e, zero voltage switching. During T_2, the inductance current I_{L_f} charges C_{snub} and V_x increases to Vdd. Similarly during T_1, the inductance current I_{L_f} discharges C_{snub} and V_x decreases to zero.

One can see that the conditions to achieve ZVS are very restrictive. Parameters have to be re-tuned when loading current changes. Design-time ZVS techniques without feedback are vulnerable to variations of devices and loading.

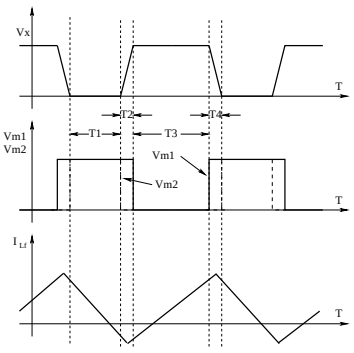

Figure 6: Conditions to achieve zero voltage switching.

4.2 Real-time ZVS technique

Assuming V_{ctrl} as the control signal of the power transistors, without considering ZVS, the control signals for the PMOS power transistor, M_1, and NMOS power transistor, M_2, are the same as V_{ctrl}, i.e.,

$$V_{m1} = V_{m2} = V_{ctrl}. \quad (8)$$

To achieve ZVS, V_{m1} and V_{m2} can be expressed as

$$V_{m1} = V_{ctrl} + \overline{V_x}, \quad (9)$$

and

$$V_{m2} = V_{ctrl} \cdot \overline{V_x}, \quad (10)$$

where V_x is the output voltage level of the power transistors. Equation (9) ensures that V_{m1} is 1 whenever V_x is 0, which implies that M_1 turns on (V_{m1} changes from 1 to 0) only when V_x is 1, i.e., the voltage drop between the source and drain of M_1 is zero. Similarly, (10) ensures that V_{m2} is 0 whenever V_x is 1, which implies that M_2 turns on (V_{m2} changes from 0 to 1) only when V_x is 0, i.e., the voltage drop between the source and drain of M_2 is zero.

Equation (9) and (10) explain the principle to achieve ZVS. The implementation of this principle, however, needs more careful analysis. To ensure that V_x stays at the perfect Vdd/zero level when M_1 and M_2 start to open, we use voltage comparators instead of inverters to implement $\overline{V_x}$ as shown in Figure 2. To drive M_1, V_x is compared with $V_{high} = VDD - \Delta v$ and only when V_x is is higher than V_{high} M_1 can open. Similarly, to drive M_2, V_x is compared with a low voltage level $V_{low} = \Delta v$ and only when V_x is lower than V_{low}, M_2 can open. In order to reduce the overshoot on V_x, we use a Δv slightly larger than zero (0.3v). However, as shown in our experiment results, it is impossible to fully eliminate overshoot.

Overall, the real-time ZVS scheme presented as part of this design is very unique in the fact that it does not rely on manually calculating the duty cycle delays for a particular design. Although there are designs that do automatic ZVS control, they do not meet the power and area requirements for on-chip high frequency applications [8, 9].

4.3 ZVS startup detection

Initially, when the circuit is cold started, there is a period of time where the output signals have abnormally large variation. During this startup period there is no need to turn on the automatic ZVS calibration control for the system. In order to avoid tuning ZVS during the startup period, a series of D flip-flops are used as delay elements to prevent the startup of the ZVS calibration scheme until after the initial transient spikes, as shown in Fig. 2.

5. EXPERIMENT RESULTS

5.1 Close loop design and analysis

To verify the idea that the output voltage ripple is proportional to the smallest duty cycle change ΔD, we have implemented the voltage comparator, as in Figure 3, at two different clock rates. One voltage comparator operates at 400MHz and the other at 1.6 GHz frequencies. We compare the output voltage ripple of the PWM buck converters implemented with these two comparators in Figure 5. Note that 130nm technology is used, the Vdd voltage is 1.3 Volt, and the reference voltage level is 0.85 Volt. As shown in the figure, the voltage ripple of the 400 MHz comparator is about 11.7% as compared to the reference voltage, while the voltage ripple of the 1.6 GHz comparator is 2.9%. By increasing the frequency of the comparator by 4X, we notice a reduction in ripple by around 4X. These experiment results show that when designing the closed loop PWM buck converter, the elements of the closed loop need to be carefully considered so that the output voltage ripple is minimized.

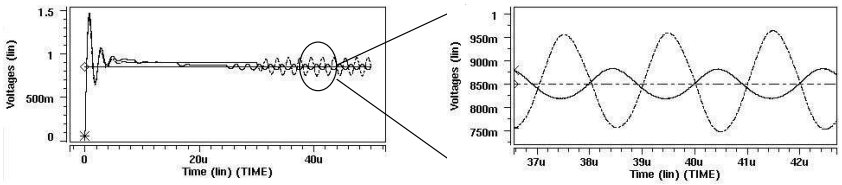

Figure 5: Comparison of voltage ripple between buck converters implemented by a 0.4GHZ voltage comparator and 1.6GHz voltage comparator.

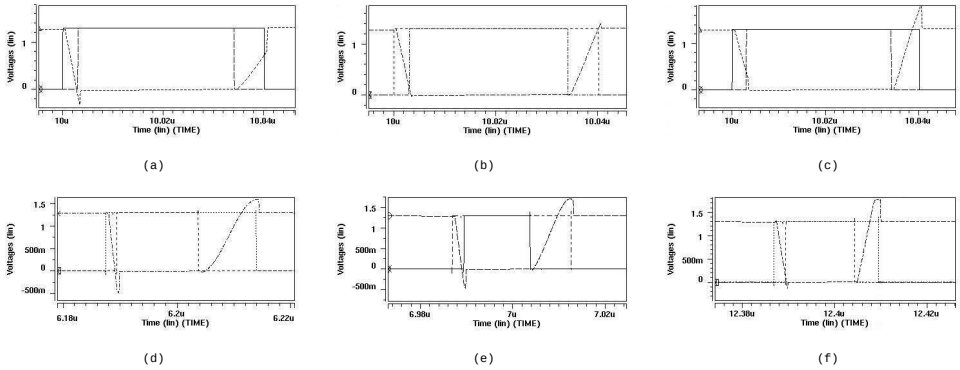

Figure 7: Design-time ZVS under loading of 5 ohms (a), 10 ohms (b), and 50 ohms (c) and real-time ZVS with feedback loop under loading of 5 ohms (d), 10 ohms (e), and 50 ohms (f). (A) and (c) fails ZVS.

5.2 ZVS control

One of the strong points of the design presented in this paper is the fact that the power of the transistors is consistent over a multitude of loads. This is mainly due to the fact that there is a real-time ZVS control system established in the circuit.

Figure 7 contains a comparison between design-time ZVS without feedback and real-time ZVS with feedback. In the case of the load of 5 and 50 ohms with design-time ZVS, one can see that the circuit is out of the ZVS mode of operation. With a load of 5 ohms, the C_{snub} capacitor is charged too slow and the voltage of V_x does not transition from the lower state to the higher state before the M_1 transistor switches on. On the other hand with a load of 50 ohms, the design-time ZVS circuit discharges the C_{snub} too slowly and the circuit is in a non optimal energy efficiency state once again. The real-time circuit always stays in the ZVS mode of operation with the various loads. Although, there is an overshoot (refer to Section 4.2) for the real-time ZVS circuit, this does not affect the energy usage of the power transistors.

Overall, not having a proper ZVS control system will cause problems in terms of power usage of the switch transistors. In terms of overall power efficiency of the circuit, both ZVS operation and the actual magnitude of the current through the load play significant roles. But our experiments show that if the proper load current is used with real-time ZVS, power efficiencies are greater than 90% consistently for various loads.

6. CONCLUSION

In this paper, we have designed a novel PWM circuit that can be used to provide a range of Vdd levels for a variety of loads by two feedback loops. With the use of an inner feedback loop between the output and input of the power transistors, we are able to ensure real-time zero voltage switching. This enables the reduction of power consumed by these transistors and achieves power efficiencies over 90% for a variety of loads. Also, an outer feedback loop is employed in the PWM circuit to track the reference voltage level. We show that this closed loop should be propriately modeled and designed to ensure a low output voltage ripple.

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